

FIG. 2(A)

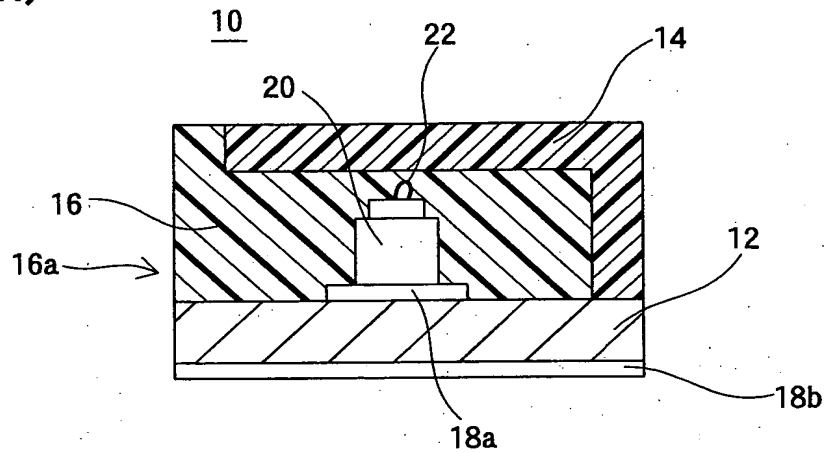


FIG. 2(B)

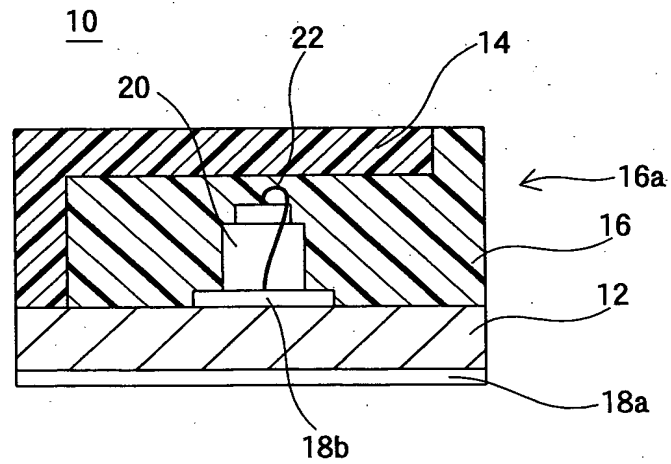


FIG. 3(A)

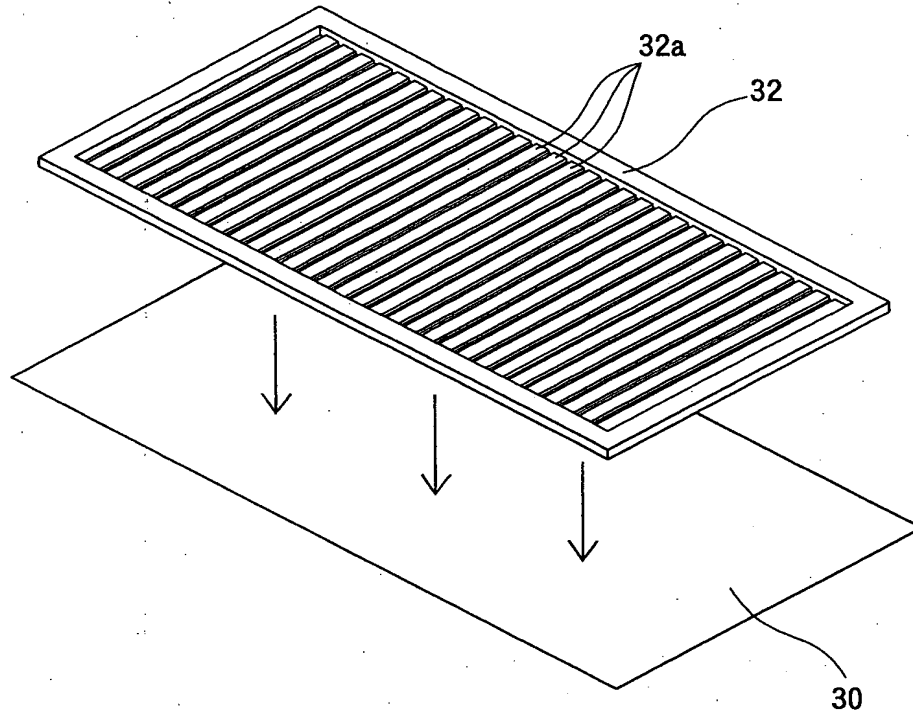


FIG. 3(B)

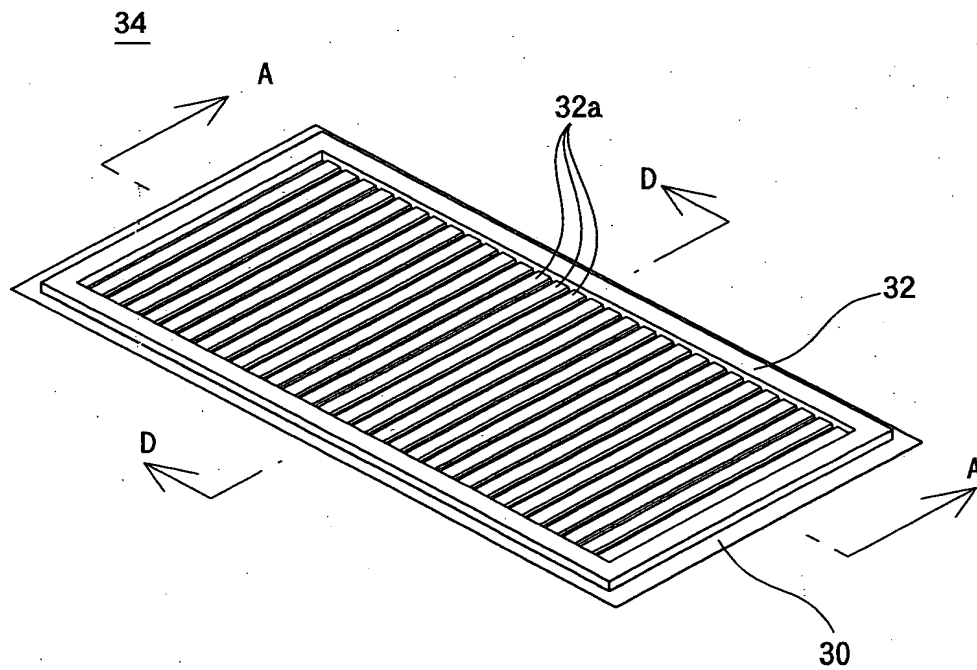


FIG. 4(A)

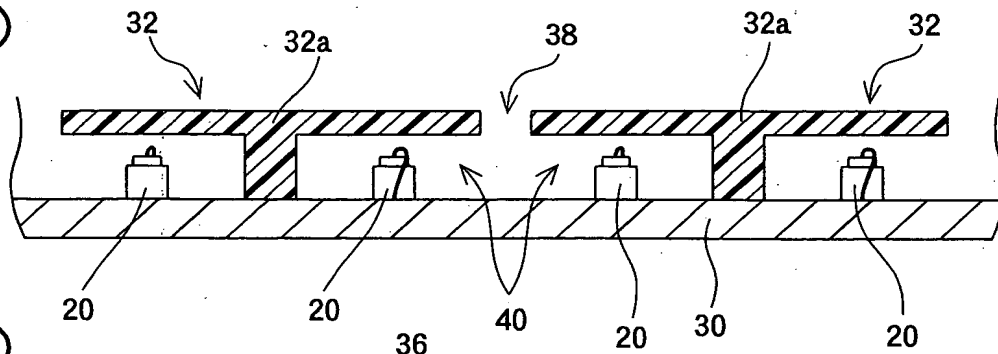


FIG. 4(B)

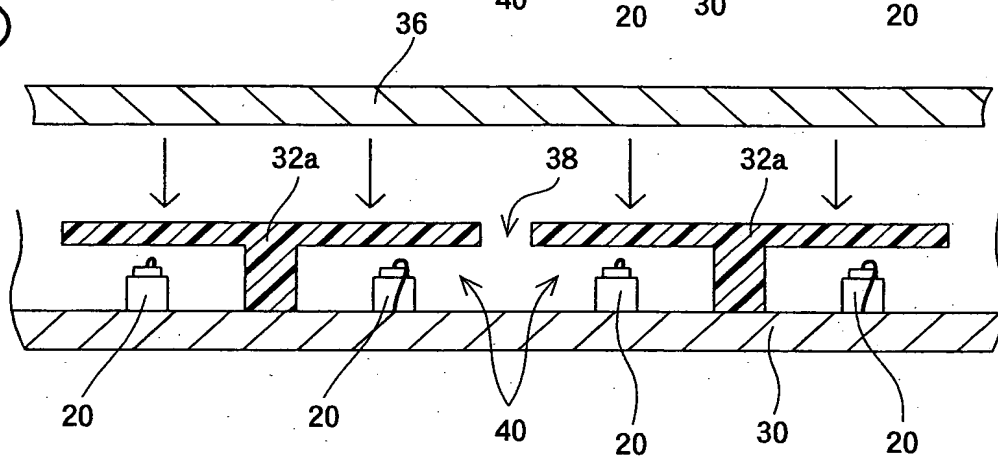


FIG. 4(C)

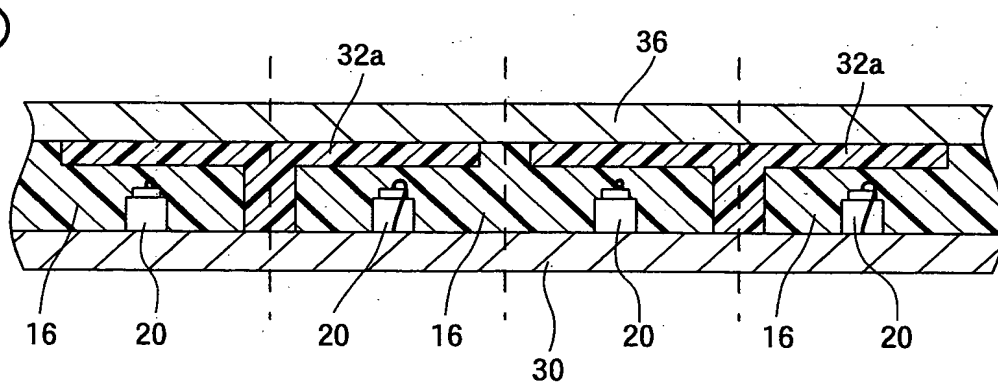


FIG. 4(D)

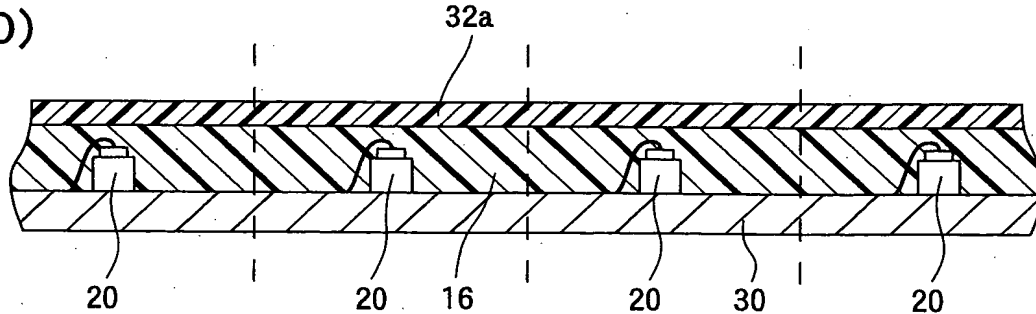


FIG. 5

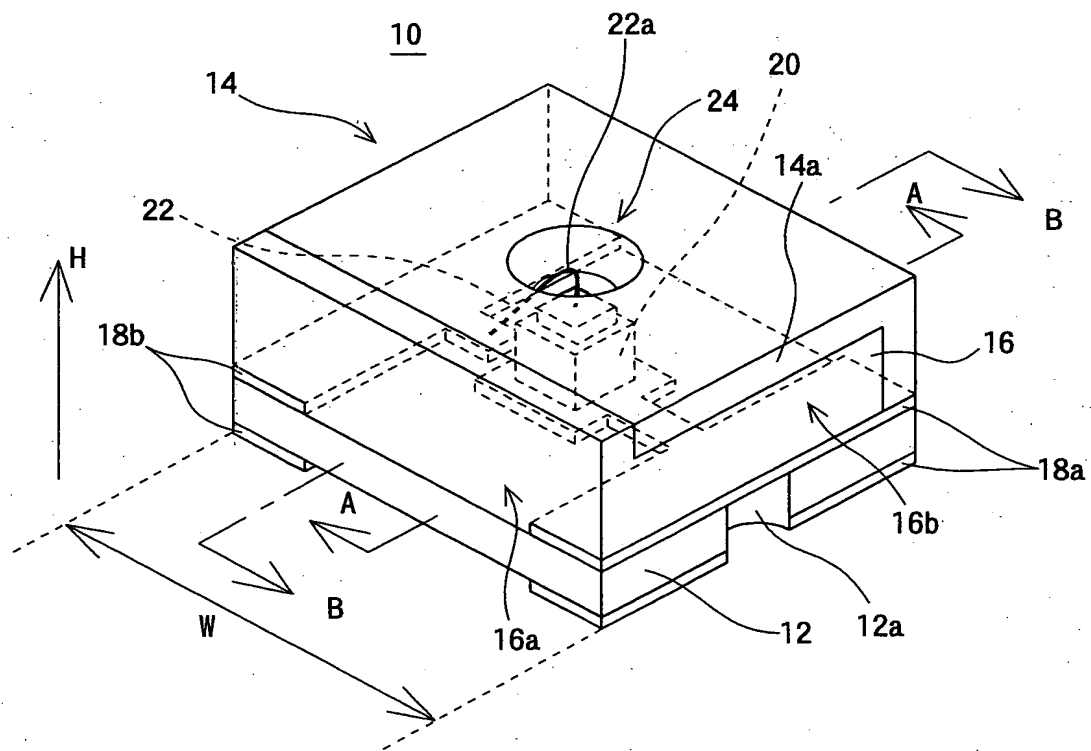


FIG. 6(A)

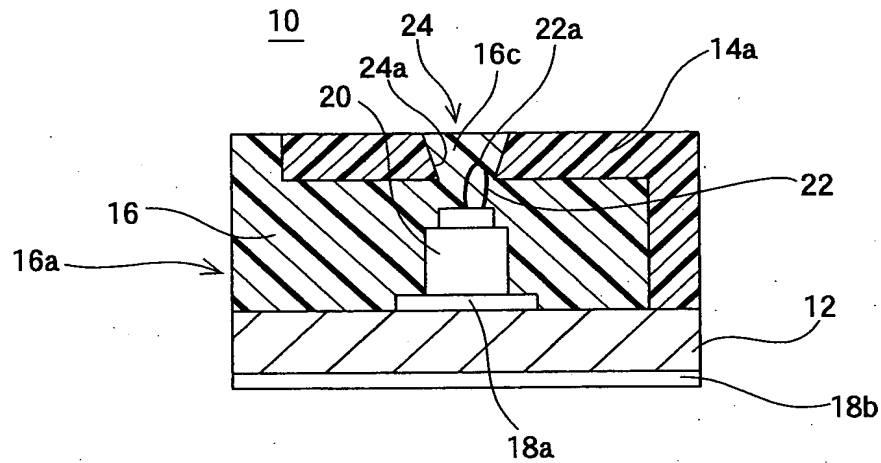


FIG. 6(B)

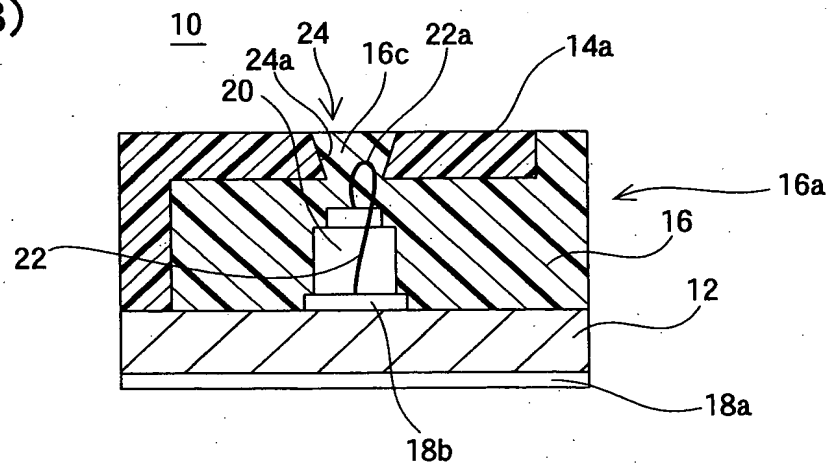


FIG. 7(A)

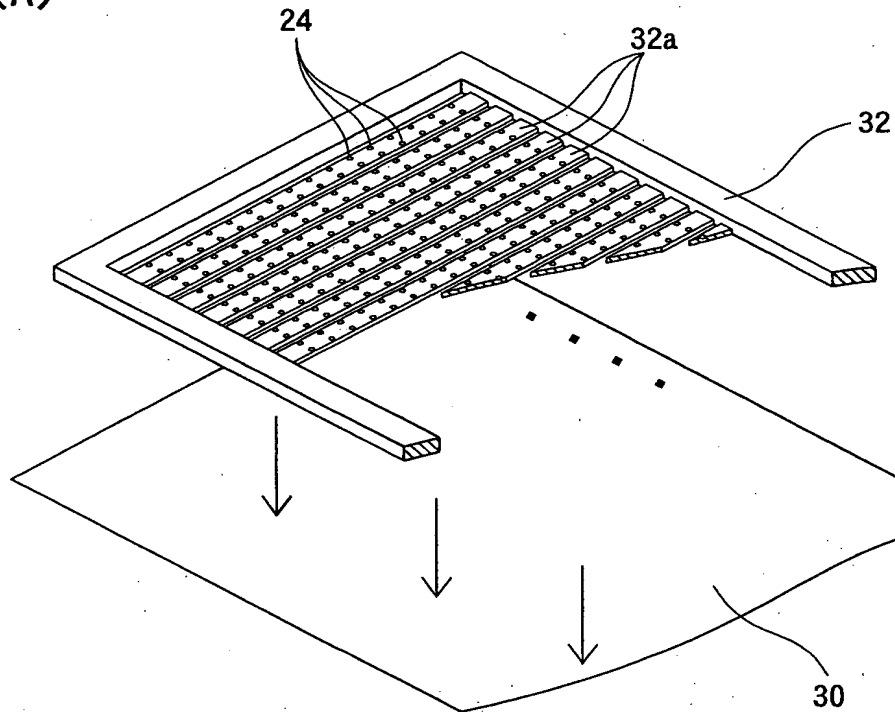


FIG. 7(B)

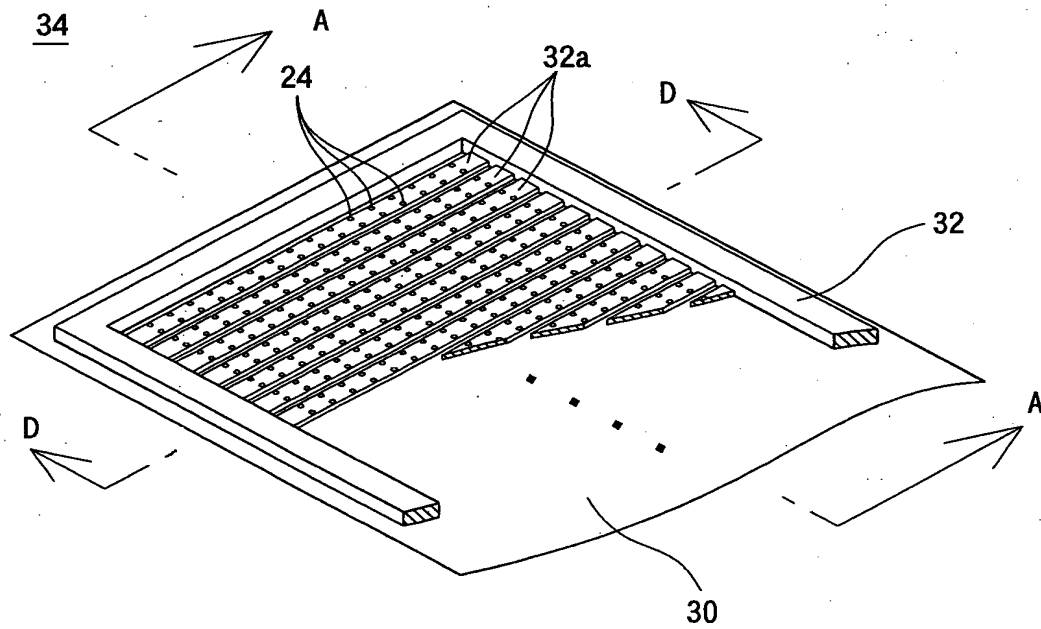


FIG. 8(A)

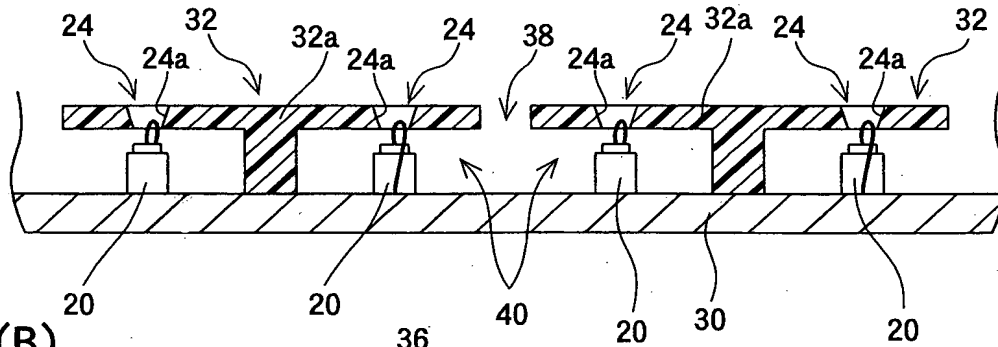


FIG. 8(B)

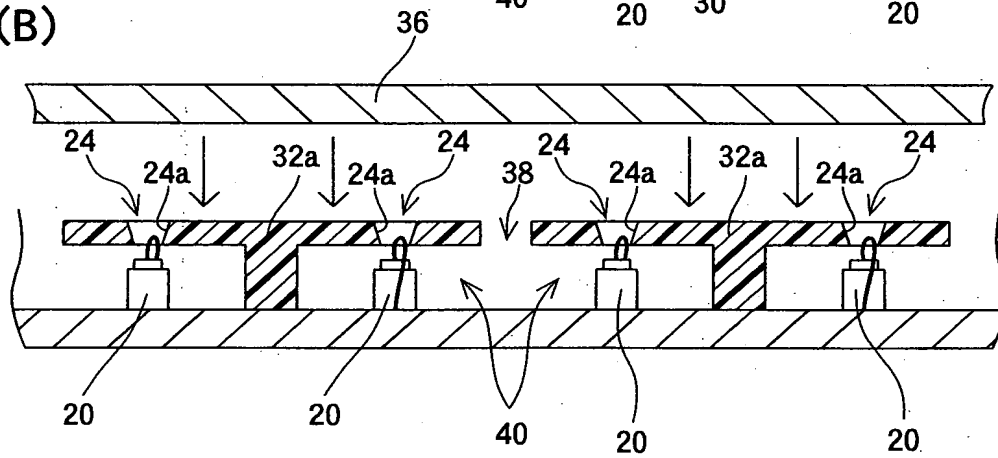


FIG. 8(C)

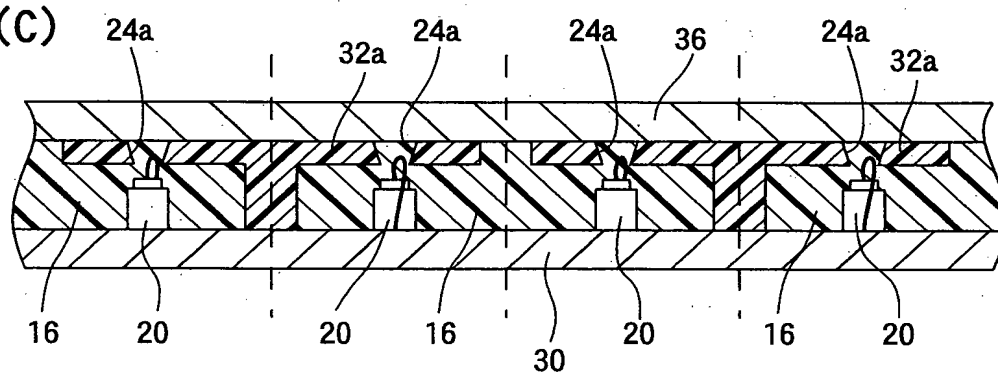


FIG. 8(D)

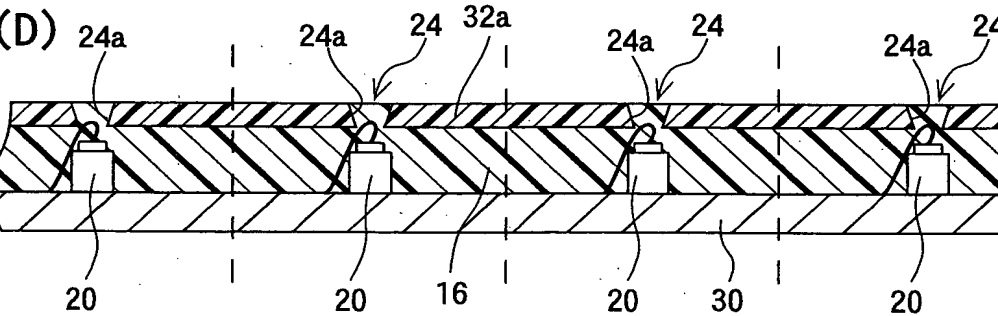


FIG. 9

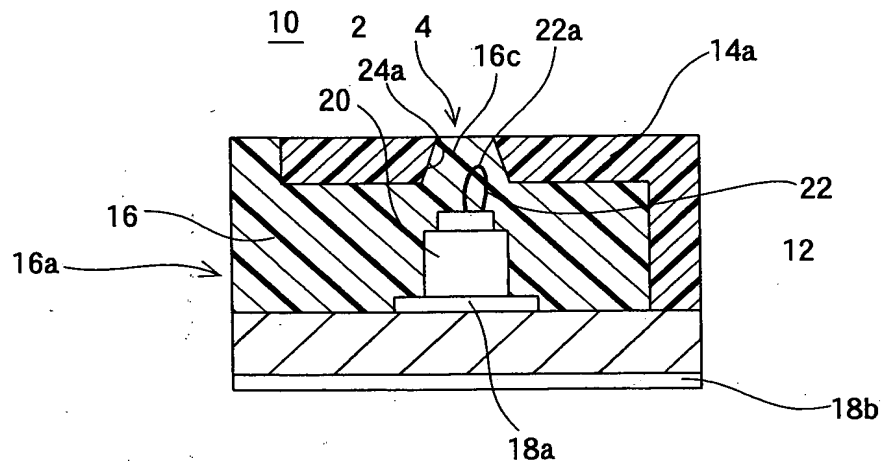


FIG. 10

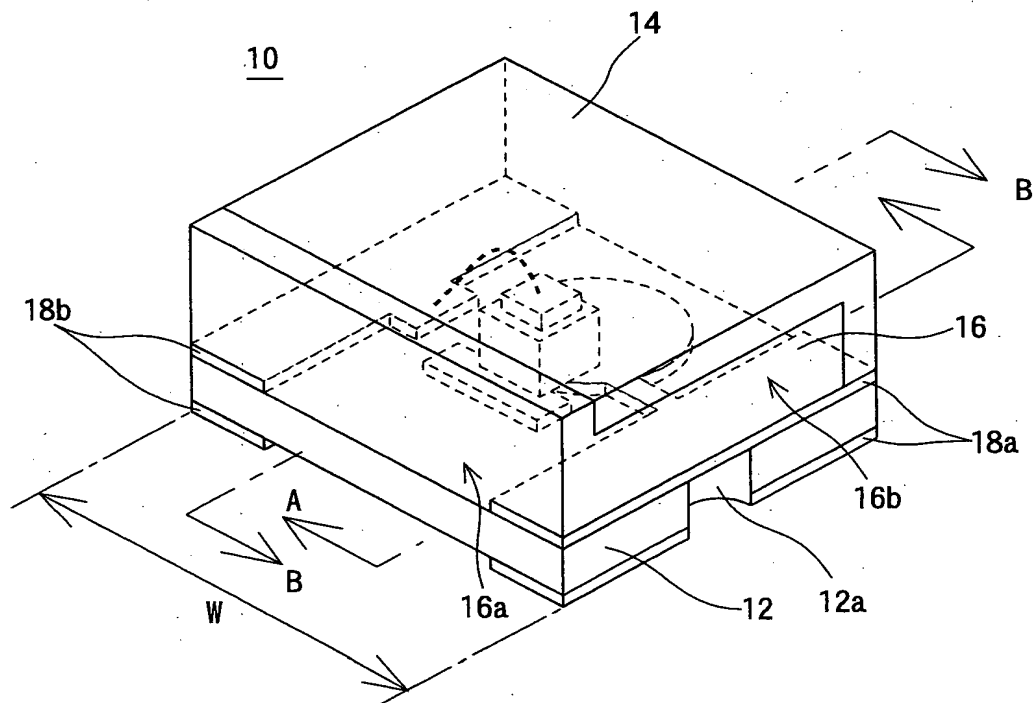


FIG. 11(A)

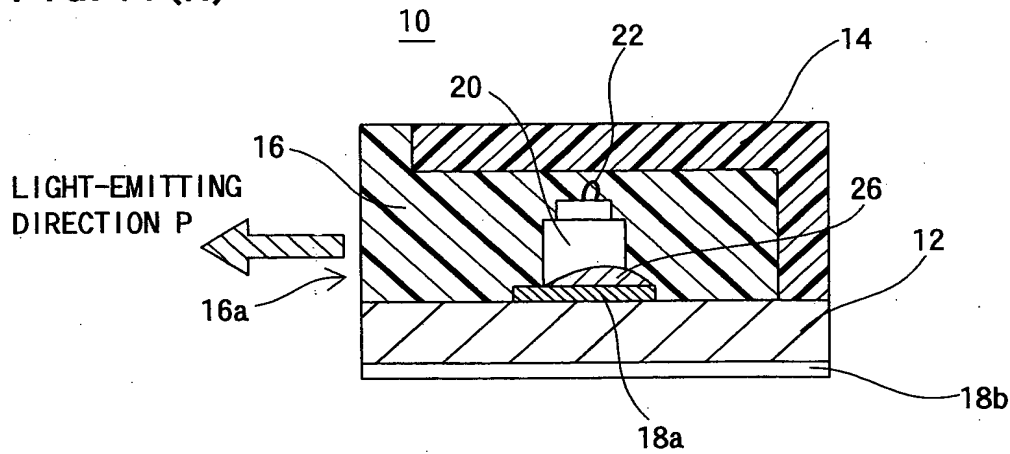


FIG. 11(B)

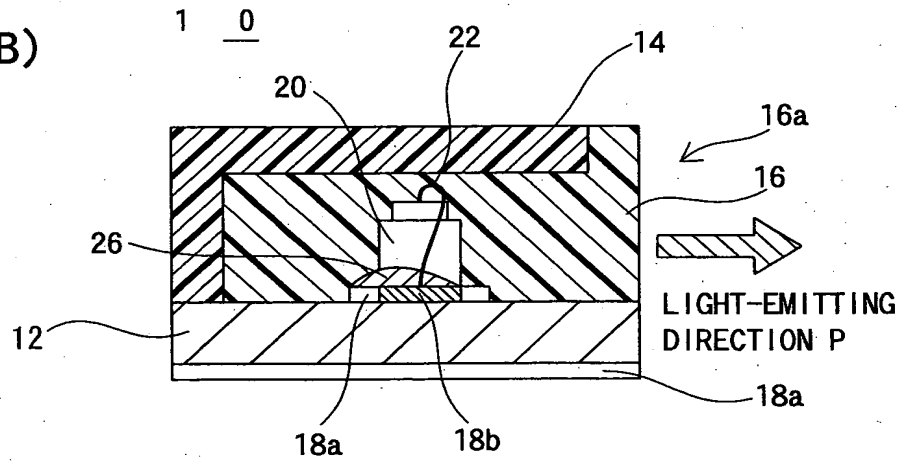


FIG. 12

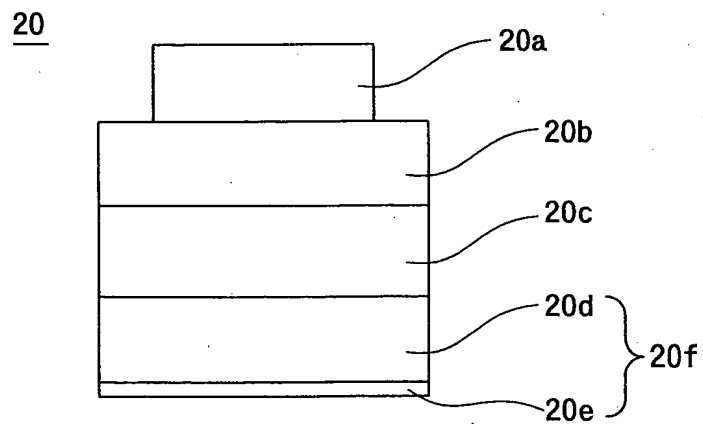


FIG. 13(A)

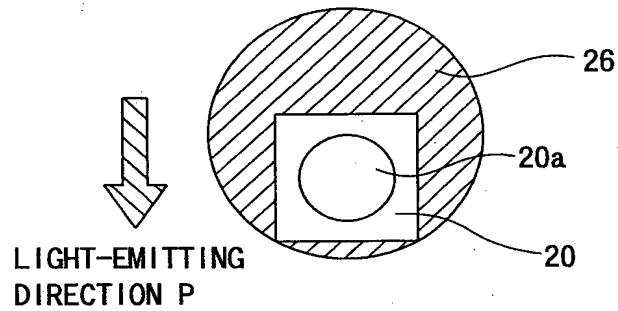


FIG. 13(B)

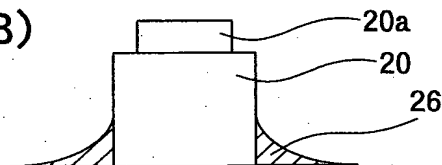


FIG. 13(C)

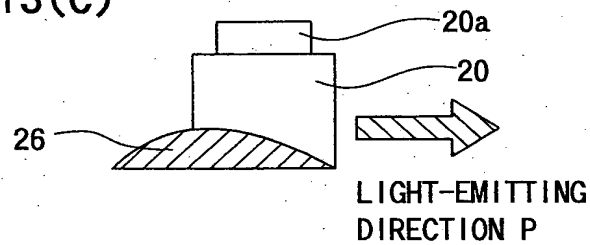


FIG. 13(D)

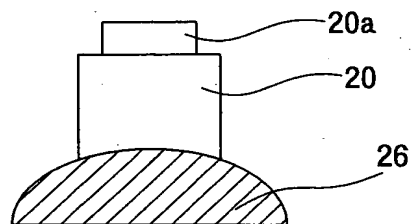


FIG. 14(A)

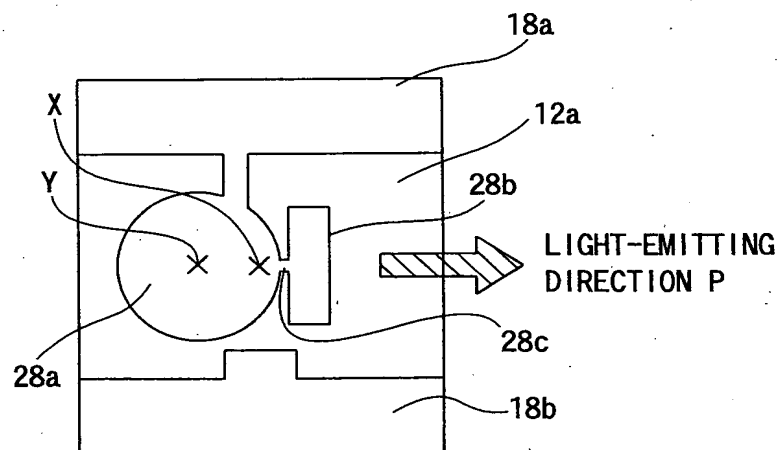


FIG. 14(B)

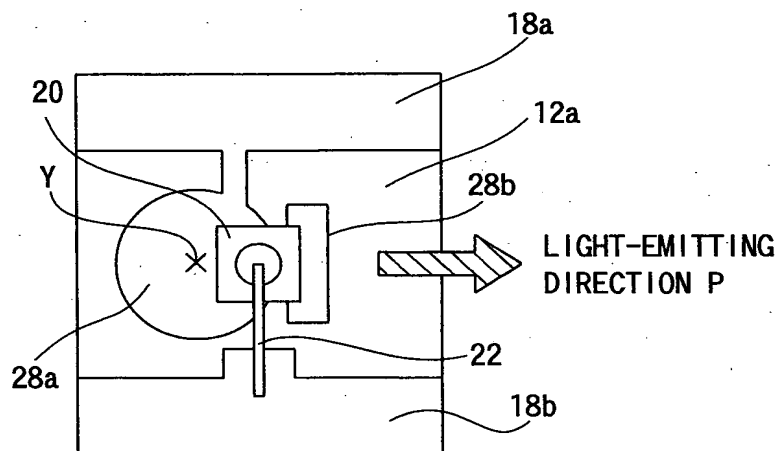


FIG. 15(A)

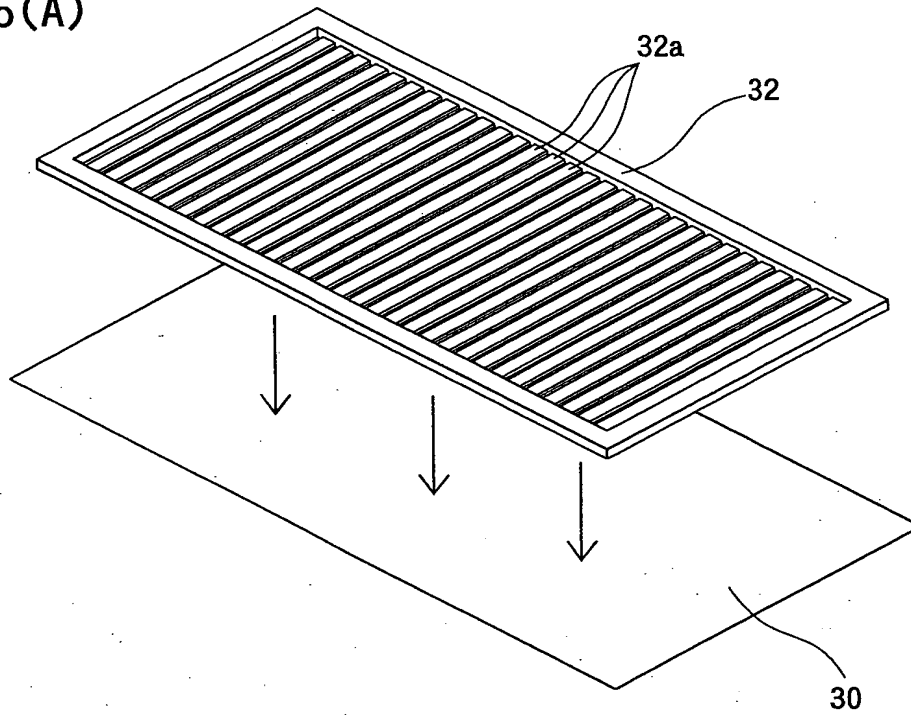
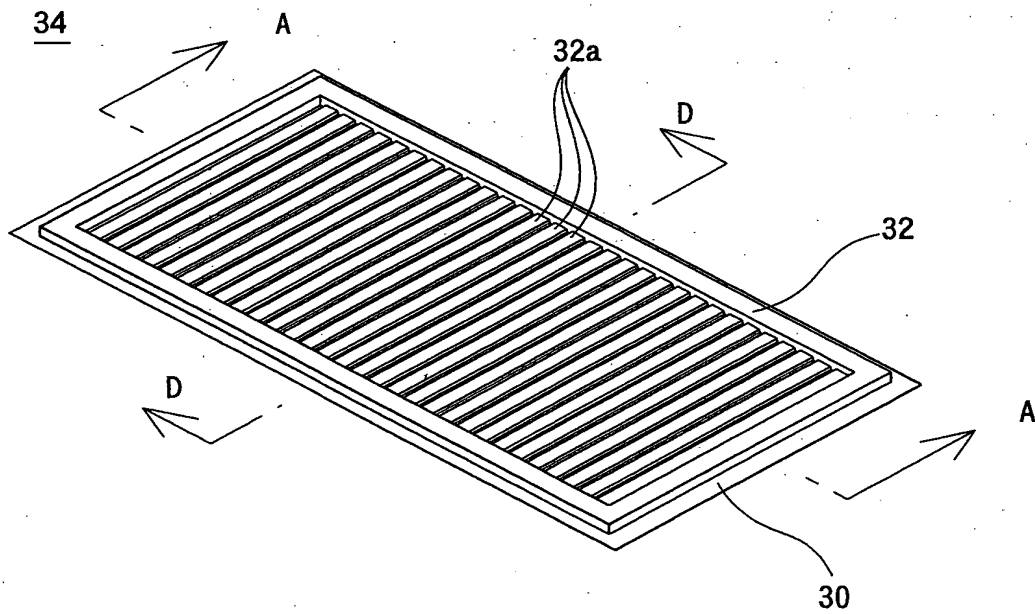


FIG. 15(B)



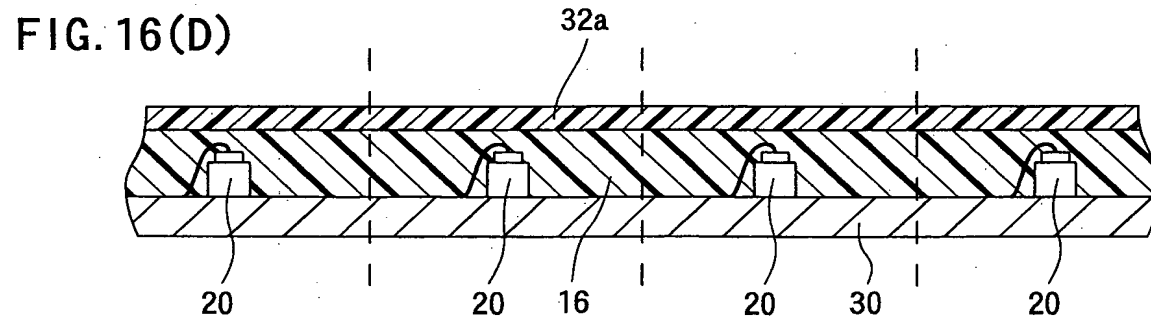
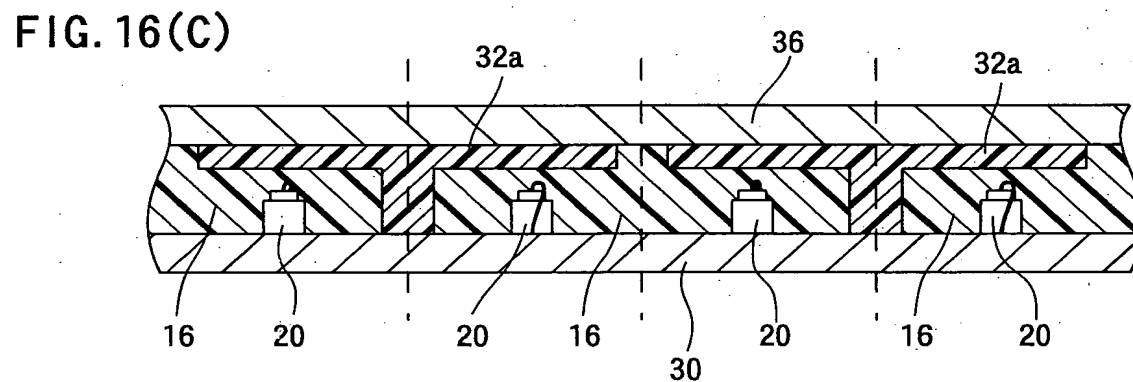
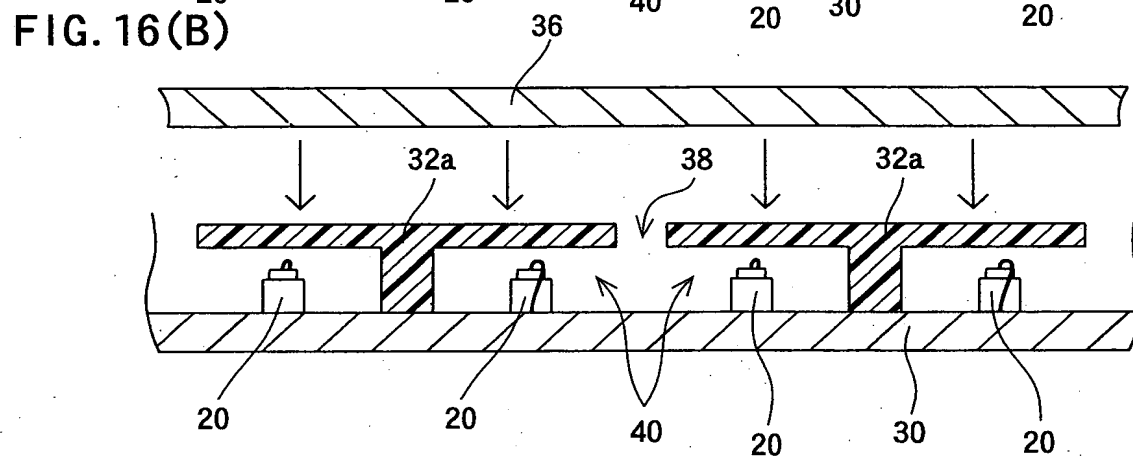
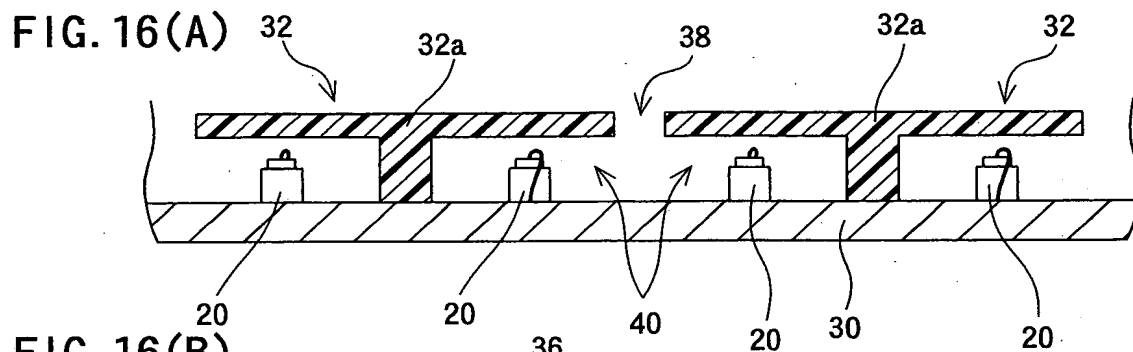


Figure 41 is a cross-sectional view of a semiconductor device 41. The device includes a substrate 42 with a top surface 42a and a bottom surface 42b. A layer 43 is formed on the top surface 42a. A structure 44 is formed on the top surface 42a, and a layer 45 is formed on the top surface 42a. A layer 46 is formed on the top surface 42a, and a layer 43a is formed on the top surface 42a.

FIG. 18(A)

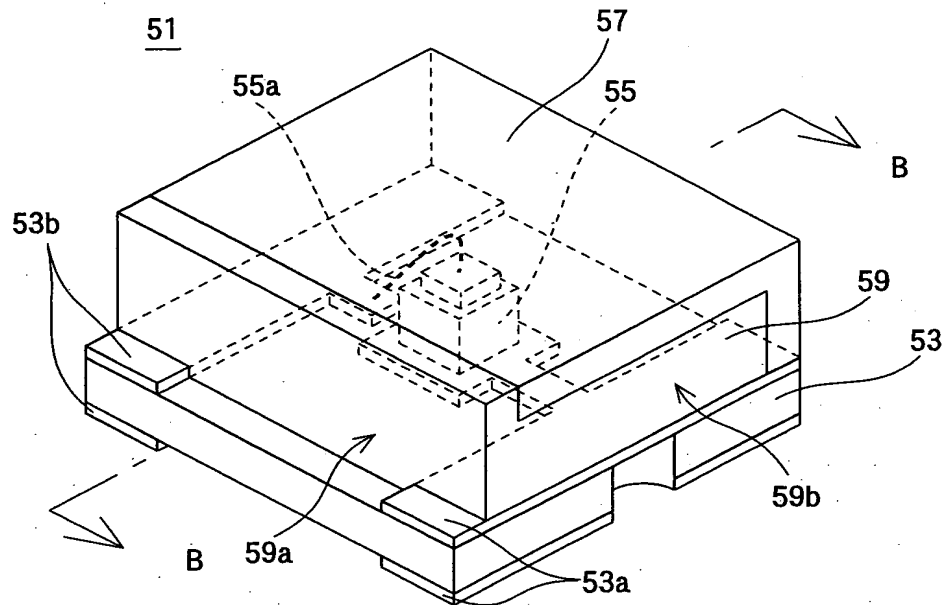


FIG. 18(B)

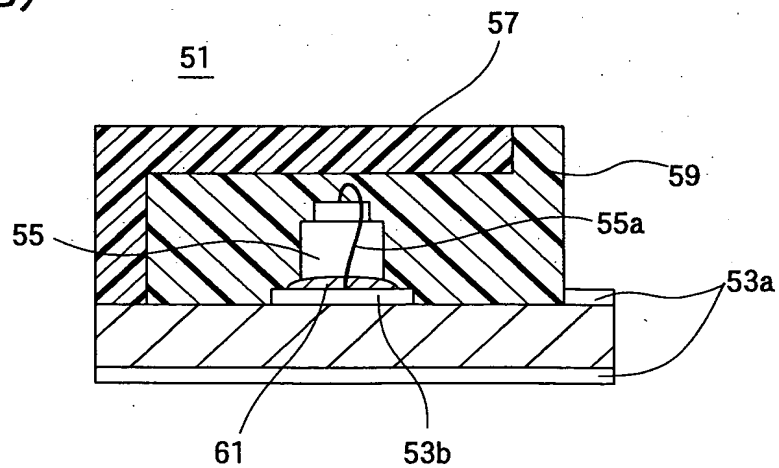


FIG. 19(A)

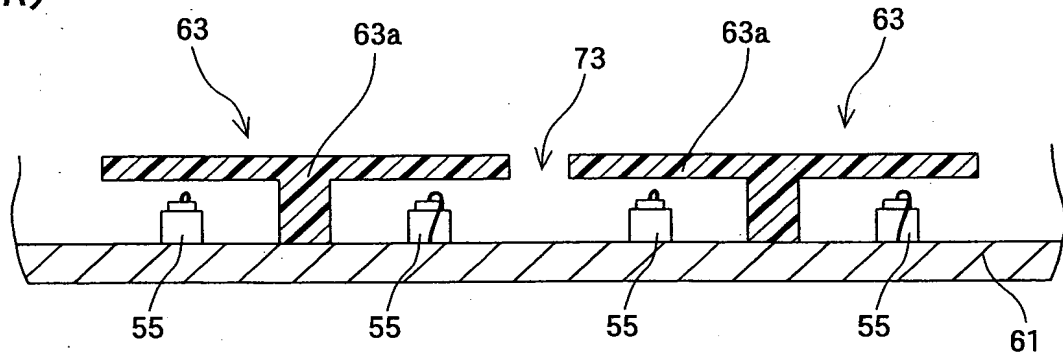


FIG. 19(B)

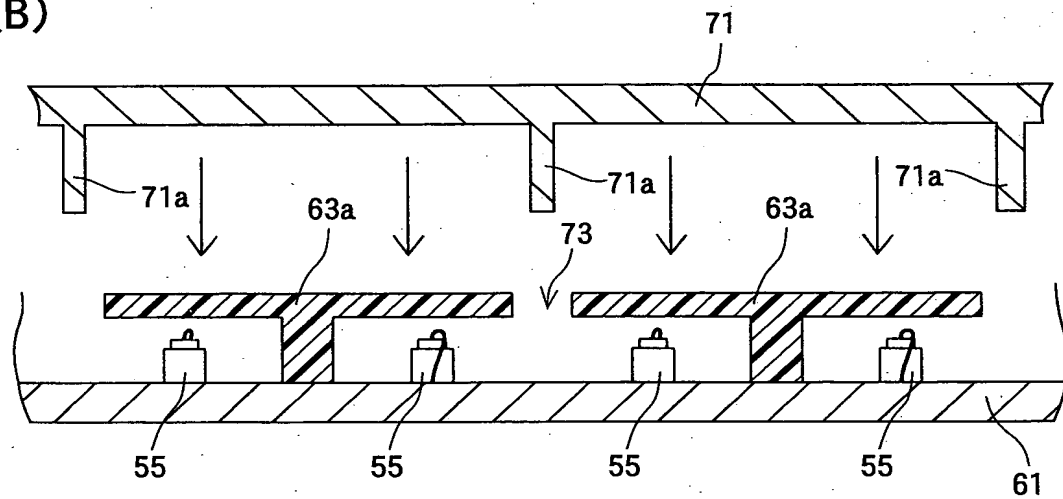


FIG. 19(C)

